DIGITAL OUTPUT CARD

MODEL 69331A

OPERATING AND SERVICE MANUAL

FOR CARDS DESIGNATED RUN 1 AND ABOVE*

*For Cards above Run 1
a change page may be
included.

100 Locust Avenue, Berkeley Heights, New Jersey 07922

HP Part No. 69331-90001

Printed: March, 1971

SECTION I
GENERAL INFORMATION

1-1 INTRODUCTION

1-2 This instruction manual contains operating and service instructions for TTL Output Card Model 69331A. The card is designed specifically for use in 6936A Multiprogrammer and 6937A Multiprogrammer Extender units to provide 12 separate TTL/DTL logic-level outputs that reflect the status of 12 programmed bits. The outputs of the standard 69331A card have ground-true logic sense (0 volt output for programmed binary 1) and TTL/DTL logic levels (0 to +5 volts). Through a simple modification, the user can change the logic level outputs to 0 to +12 volts or operate the output transistors as open collector drivers.

1-3 By employing Option 073 of the 69331A, the logic sense of the 12 output signals can be reversed (+5 volt output for a programmed binary 1). See Paragraph 1-17 for details on Option 073.

1-4 Overall system concepts, including system installation, troubleshooting, and operating considerations are covered in the instruction manual for the 6936A Master unit and will not be repeated in this manual.

1-5 DESCRIPTION

1-6 When installed in a multiprogrammer system, the TTL output card is programmed by a 16-bit word originating at a remote computer or the 6936A Multiprogrammer control panel. Twelve of the programmed bits represent data while the remaining four contain the slot address of the output card.

1-7 When the card is addressed and strobed, the 12 data bits are stored in flip-flop registers on the card. If the system enable (SYE) mode is programmed on, the stored data is passed through a set of AND gates to 12 individual output driver circuits. The logic signal outputs of the drivers are then coupled directly to the card output connector.

1-8 The TTL output card also contains an SYE circuit and a gate/flag circuit. The SYE circuit holds the 12 output logic lines in the 0-state (all bits HI for the standard 69331A and all bits LO for Option 073) until SYE is programmed on. The gate/flag circuit, which is controlled by the data transfer enable (DTE) bit, can be used to signal the external system (via a transition of the output gate signal) that new data is available on the 12 output data lines. A flag return signal from the external device will hold the common timing flag ($\overline{\text{CTF}}$) signal returned to the multiprogrammer in the "busy" state until the external system has completed its input cycle. The detailed functions of these circuits are covered in Sections III and IV of this instruction manual.

1-9 The output card is fabricated on a $4\frac{1}{2}$" x 11" printed circuit card. The inner edge of the card contains a dual 24 pin (48 pin total) printed circuit plug that can mate with any connector in slot 400 through 414 of a multiprogrammer unit (6936A or 6937A). A dual 15-pin (30-pin total) printed circuit plug located on the outer-edge of the card connects the 69331A outputs to the external device.

1-10 SPECIFICATIONS

1-11 Table 1-1 provides detailed specifications for the Model 69331A.

1-12 INTERFACING

1-13 The 69331A TTL Output Card is automatically interfaced with its associated multiprogrammer unit when it is installed in a 400 series slot connector. Once it is assigned to a slot, the card assumes the address of that position and will receive programmed data only when the applicable unit and slot are addressed. All operating power and programmed data for the card are derived from the multiprogrammer unit.

1-14 Interfacing considerations involving the 69331A and the external device are covered in detail in Section III of this Instruction Manual.

1-15 OUTPUT CONNECTOR ASSEMBLY

1-16 One 30-pin output connector assembly (HP Part No. 5060-7934) is furnished with each TTL output card for interfacing the output card with the external system. Additional 30-pin connector assemblies may be ordered from your local Hewlett-Packard sales office (refer to list at rear of manual for addresses).

1-17 OPTIONS

1-18 Option 073 of the 69331A reverses the logic sense relationship between the programmed data

bits and the card output bits from the standard ground-"true" logic sense to the +5 volt-"true" logic sense. With this option, a binary 1 programmed at the computer will cause the corresponding output bit of the 69331A to go to the +5 volt (HI) logic level. The option is implemented by simply replacing plug-in IC AND gates (HP Part No. 1820-0141) Z7, Z8, and Z9 with plug-in IC NAND gates (HP Part No. 1820-0054). The physical locations of Z7, Z8, and Z9 are shown on the component location diagram of Figure 7-1.

1-19 The schematic diagram of the standard 69331A also applies to the Option 073 circuit, with the following exceptions:

a. The AND gate symbols for Z7, Z8, and Z9 change to NAND gate symbols (all IC pin numbers remain the same).

b. The Mnemonics for the output bits of the card change from $\overline{B--}$ to B--.

1-20 ORDERING ADDITIONAL MANUALS

1-21 Two manuals are shipped with each 69331A order. Additional manuals may be purchased from your local Hewlett-Packard field office (see list at rear of this manual for addresses). Specify the card model number and HP Part Number shown on the title page.

Table 1-1. Model 69331A Specifications

DATA INPUT:
12 bit binary. Programmed binary 1 = output in LO state; programmed binary 0 = output in HI state. (Option 073 reverses this relationship.)

OUTPUT LEVELS:
Standard: LO = 0 to +0.3V (32mA max. sink current); HI = +4.5V to +5.0V (1 kilohm source impedance).
User-connected options: 0 to +12V (nominal) logic levels or open collector drivers.

DEVICE COMMAND (GATE) OUTPUT:
One normally HI or normally LO (user selectable) logic level line. Change in level indicates data is present on card output. Level reverts to original status either at start or end (user selectable) of external device response period.

DEVICE SIGNAL (FLAG) INPUT:
LO: 0 to +0.5Vdc; I_{source} of 15mA maximum.
HI: +2.4 to +5.0Vdc.
Minimum pulse width: 2μsec. Presence of signal (either HI or LO; user selectable) indicates external device has received data. End of signal indicates external device has completed response period. If external FLAG input signal is not desired, GATE output can be connected directly to FLAG input.

TEMPERATURE RANGE:
0°C to +80°C operating in mainframe (allows +25°C internal rise when operating in mainframe at up to +55°C ambient).
-40°C to +80°C storage.

SYSTEM ENABLE FUNCTION:
All outputs are held at logical 0 until system enable bit is programmed.

OPERATING POSITION:
Any (no restrictions).

OUTPUT CONNECTOR:
One 15 pin dual (30 pin total) edge connector. Mating female connector assembly supplied (HP Part No. 5060-7934).

DIMENSIONS:
4.5" x 11.0" nominal.

WEIGHT:
0.7 lbs.

SECTION II
INSTALLATION

2-1 INITIAL INSPECTION

2-2 Before shipment, the 69331A TTL Output Card was inspected and found to be free of mechanical and electrical defects. As soon as the card is received, proceed as instructed in the following paragraphs.

2-3 MECHANICAL CHECK

2-4 If external damage to the shipping carton is evident, ask the carrier's agent to be present when the card is unpacked. Check the card for signs of physical damage. If it is damaged, file a claim with the carrier's agent and notify Hewlett-Packard Sales and Service Office as soon as possible. If it appears to be undamaged, perform the electrical check specified in the following paragraph.

2-5 ELECTRICAL CHECK

2-6 Check the electrical performance of the output card as soon as possible after receipt. Section V of this manual contains checkout procedures which will verify operation of the card. Refer to the inside front cover of this manual for Certification and Warranty statements.

2-7 REPACKING FOR SHIPMENT

2-8 When shipping an output card, it is recommended that the package designed for it be used. The original packaging material is reusable. If it is not available, contact your local Hewlett-Packard field office to obtain the materials. This office will also furnish the address of the nearest service office to which the output card can be shipped. Be sure to attach a tag to the output card specifying the owner, model number, and service required, or a brief description of the trouble.

2-9 OUTPUT CARD INSTALLATION

2-10 Output cards are installed in slots 400 through 414 of a Multiprogrammer unit. To install an output card, proceed as follows:

a. Open the hinged front panel of the Multiprogrammer unit by turning the recessed screw within the knurled handle counterclockwise.

b. With the extractor handle on the top and the card components on the right, slide the card into the desired output slot (400 through 414). Note that all output cards are slotted between pins 4 and 5 and all 400 series connectors of the Multiprogrammer are keyed between the same points. This makes it virtually impossible to plug an output card in upside down or into any slot other than a 400 series slot.

c. Route all wiring from the output cards through the false-bottom channel and out the back of the unit to the external system.

d. As physical installation and wiring are completed for the output card, carefully note and record the following types of information on the installation record card located on the rear of the hinged front panel of the multiprogrammer.

(1) Output card type
(2) Application in external system
(3) Timing flag period, logic sense, etc.

SECTION III
OPERATING INSTRUCTIONS

3-1 DATA INPUT

3-2 The TTL output card is controlled by the multiprogrammer unit in which it is installed. All dc operating power, address and data bits, and control signals are supplied to the output card through multiprogrammer main frame connectors in slots 400 through 414. Figure 3-1 illustrates the signals present on all multiprogrammer 400-series connectors.

3-3 PROGRAMMING

3-4 The programming information presented here defines the relationships between programmed data and the 69331A card outputs. Complete system programming instructions are given in the Operating and Service Manual for the 6936A Multiprogrammer.

3-5 There are four general steps involved in programming a TTL output card. They are:

a. Addressing the multiprogrammer unit and slot containing the output card.

b. Programming a data word that will produce the desired output bit patterns.

c. Enabling the output card by programming the system enable (SYE) bit to a logical 1.

d. Programming the data transfer enable (DTE) mode, which will generate a GATE signal to the external system.

3-6 It is assumed in the following discussion that the reader is familiar with the definitions and functions of multiprogrammer control and data words. If this is not the case, it is suggested that Section III of the 6936A Instruction Manual be reviewed before proceeding.

3-7 SYSTEM ENABLE

3-8 An SYE control line is wired to all multiprogrammer 400 series slots. When the system enable function is programmed as part of a control word, the SYE line goes HI. This enables a set of 12 logic gates which pass the data bits stored in the card flip-flop registers to the output driver circuits. Prior to SYE being programmed, all output bits are held in the logical 0 state of the external device (all bits HI for the standard 69331A; all bits LO for Option 073).

3-9 The SYE control line has a second function

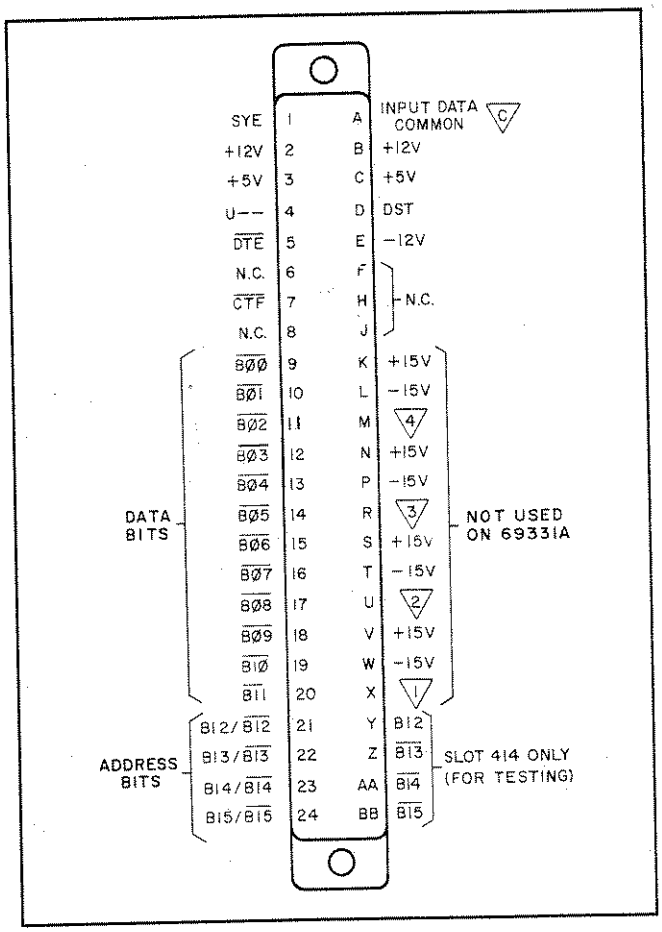


Figure 3-1. Multiprogrammer 400 Series Slot Connector

on the 69331A; that is to inhibit the GATE output to the external device until the system enable mode is programmed. This feature prevents a GATE from being generated during initialization.

3-10 ADDRESSING

3-11 An output card is selected to receive new data when its associated address bits (B12/$\overline{B12}$ through B15/$\overline{B15}$) and a unit select line U--) are all HI. Although both the true and complemented forms of the address bits are represented on Figure 3-1 (e. g. B12 and $\overline{B12}$) only one of the two states is present on each of the four address gate lines when the card is installed in a multiprogrammer slot. For example, if the output card is installed in slot 405, then bits B12 (1), $\overline{B13}$ (2), B14 (4), and $\overline{B15}$ (8) will

be present on the address lines, and all four lines will be HI when slot 405 is addressed. The U-- line is HI when the associated multiprogrammer unit is selected as part of a control word. The unit selection is stored by the 6936A and it remains in effect until a different unit is selected by a later control word.

3-12 OUTPUT BITS $\overline{B\emptyset\emptyset}$ THROUGH $\overline{B11}$

3-13 Programming. Output bits $\overline{B\emptyset\emptyset}$ through $\overline{B11}$ are stored in the TTL output card storage registers when the card is addressed and strobed. If SYE has been programmed, the stored bits will be transferred through logic gates to output inverting amplifiers. The output amplifiers of the standard 69331A card will produce a LO (0 volt) output in response to a programmed binary 1 ($\overline{B--}$, LO). When Option 073 is employed, the amplifier outputs will go HI (+5 volt) for a programmed binary 1. Figure 3-2 shows the pin numbers on the TTL card output connector from which the output bits can be taken.

3-14 Output Bit Levels. As supplied from the factory, jumper J4 on the PC card is connected to pad A (+5 volts). With this connection, the output bits will switch between the following levels:
HI: +4.5V to +5V (source impedance = 1 kilohm)
LO: 0 to +0.3V (I sink = 32mA max.)

3-15 By moving jumper J4 to pad B on the PC card, the bit levels will be:
HI = +12V nominal (source impedance = 1 kilohm)
LO = 0 to +0.3V (I sink = 32mA max.)

3-16 A third user-connected option allows the output amplifiers of the TTL output card to be operated as open collector drivers. In this method of operation the 1 kilohm collector load resistors (R2) on the TTL card are removed and the external device supplies the collector voltage and load resistors. Specifications on the TTL card driver transistors are:

LO output (Q1 on) = 0 to +0.3V with max. I sink of 32mA.

HI output (Q1 off) = +30V max.

Power Dissipation of Q1 (at 80°C) = 135mW max.

3-17 DTE MODE

3-18 The primary purpose of the data transfer enable (DTE) mode is to provide a means of generating a GATE signal to the external device under program control. The GATE signal can then be used to strobe the programmed information available on the previously addressed TTL output card (or cards) into the external device, and to start a timing flag circuit in the external device that will hold the $\overline{CTF}$ line returned to the multiprogrammer in the busy

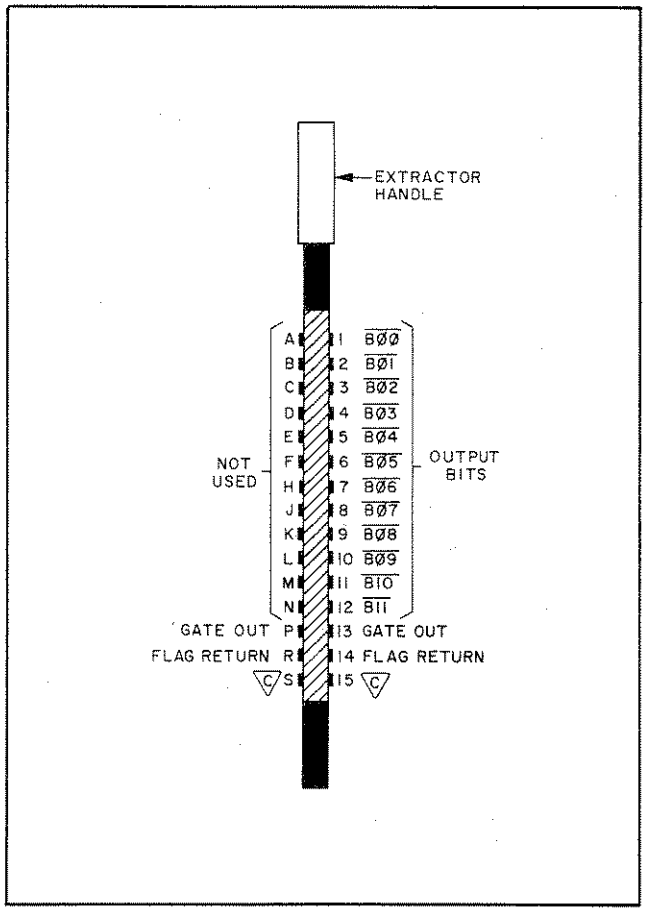


Figure 3-2. 69331A Output Connector

state until the external circuit times out.

3-19 GATE Signal. After SYE has been programmed on, two conditions must be satisfied in order to generate a GATE to the external device from a single TTL output card or from a group of TTL output cards: (1) the card (or cards) must be addressed and strobed; (2) the DTE mode must be programmed on. The first condition is stored (latched) when it occurs so that when DTE is programmed on, any previously addressed $\overline{TTL}$ output cards will generate an output GATE signal.

3-20 A second method of generating an output GATE signal is to keep DTE selected. Then, each time a particular TTL output card is addressed and strobed it will generate an output GATE.

3-21 As supplied from the factory (jumper J3 to B) the output GATE line of the TTL card will normally be HI and switch to the LO level when the two gate-enabling conditions described above are satisfied. By moving jumper J3 to A, the GATE line will normally be LO and switch HI to indicate an active GATE.

3-22 The output GATE levels are normally 0V (LO) to +5V (HI). However, the options described for the data bit drivers in Paragraph 3-14 also apply to GATE driver Q3.

3-23 External FLAG Circuit. The timing flag circuit in the external device should be started when the GATE output of the TTL card switches to the active state (LO for the standard J3-B connection and HI for the optional J3-A connection) and run for the busy-period of the external device.

3-24 The device FLAG returned to the TTL card must have the following characteristics:

LO: 0 to +0.5V (Isink = 15mA max.)

HI: +2.4 to +5.0V

FLAG PERIOD: 2μsec min (leading edge of FLAG signifies start of device busy period and trailing edge signifies end of device busy period).

FLAG LOGIC SENSE: LO-busy (standard)
HI-busy (user option; see Table 3-1).

3-25 A simplified block and timing diagram of the $\overline{\text{GATE}}$, $\overline{\text{FLAG}}$, and $\overline{\text{CTF}}$ signal functions for the STANDARD J1 and J2 strapping options and a LO-busy device $\overline{\text{FLAG}}$ are illustrated in Figure 3-3. The timing sequence for these connections are as follows:

T0 - The TTL card is addressed and strobed; DST is latched by a flip-flop.

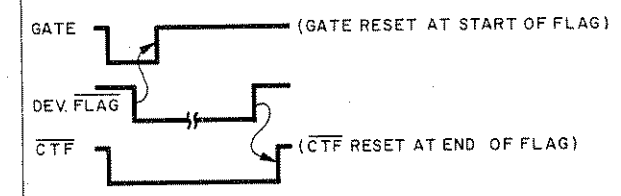
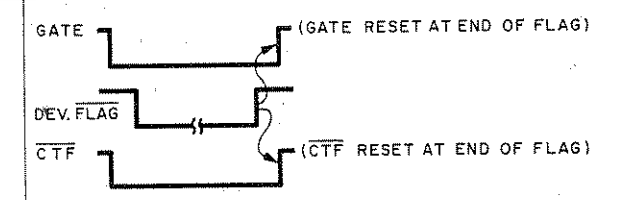
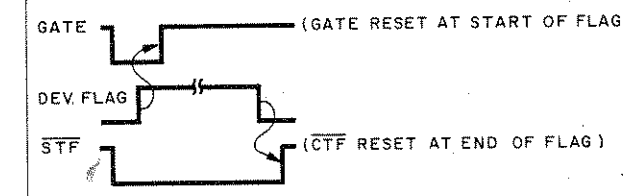
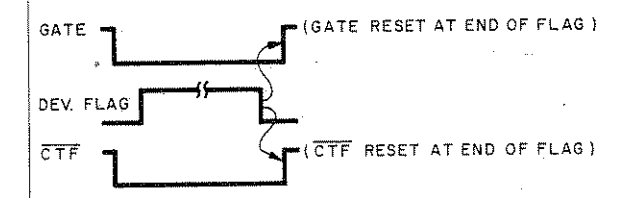
T1 - The DTE mode is programmed on. The combination of DTE and DST LATCHED sets the $\overline{\text{GATE}}$ and $\overline{\text{CTF}}$ outputs of the card to the active (LO) state.

T2 - In response to the $\overline{\text{GATE}}$ transition, the external device sets the $\overline{\text{FLAG}}$ return line to the busy (LO) state and holds it busy until it has completed its processing.

T3 - Following a short delay after the device $\overline{\text{FLAG}}$ goes busy, a negative edge detector circuit on the TTL card generates a pulse which resets the $\overline{\text{GATE}}$ line to the HI state.

T4 - The device $\overline{\text{FLAG}}$ returns to the ready (HI) state.

Table 3-1. GATE, FLAG, and $\overline{\text{CTF}}$ Timing Options

DEVICE FLAG LOGIC SENSE	JUMPER CONNECTIONS J2	JUMPER CONNECTIONS J1	GATE AND $\overline{\text{CTF}}$ TIMING RELATIVE TO DEVICE FLAG
READY / BUSY	B*	A*	
READY / BUSY	A	A	
BUSY / READY	A	B	
BUSY / READY	B	B	

* CARD SUPPLIED WITH THIS CONNECTION.

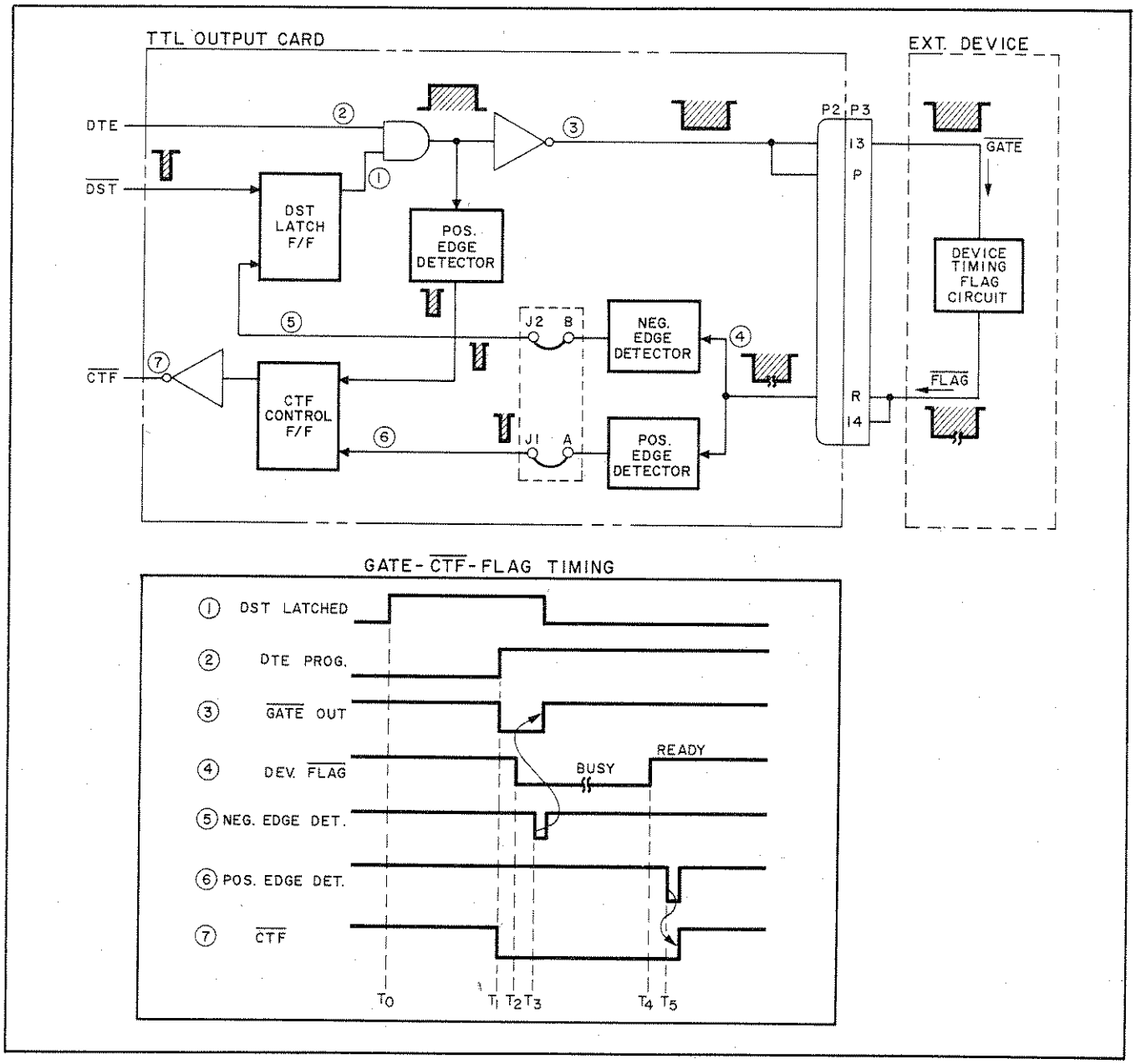


Figure 3-3. GATE/FLAG Timing Circuit, Simplified Diagram

T5 - A positive-edge detector on the TTL card generates a pulse which resets the CTF line to the ready (HI) state.

3-26 The timing relationships between the GATE, FLAG, and CTF signals for other J1 and J2 jumper options are covered in Table 3-1.

3-27 In applications where an external timing circuit is not required, the GATE output of the TTL card should be connected directly to the FLAG input of the card (Pin 13 to 14).

3-28 CABLE FABRICATION

3-29 Since the TTL output card may be used to interface with various external devices, an interconnecting cable must be prepared for the particular device being used. A 30-pin output connector is furnished with each TTL output card for this purpose. Figure 3-2 illustrates the output signals and associated connector pin numbers of the TTL output card. A 30-conductor cable (28 gauge max. wire) is required to interconnect the TTL card and the external device. The cable length should be kept as short as possible.

SECTION IV
PRINCIPLES OF OPERATION

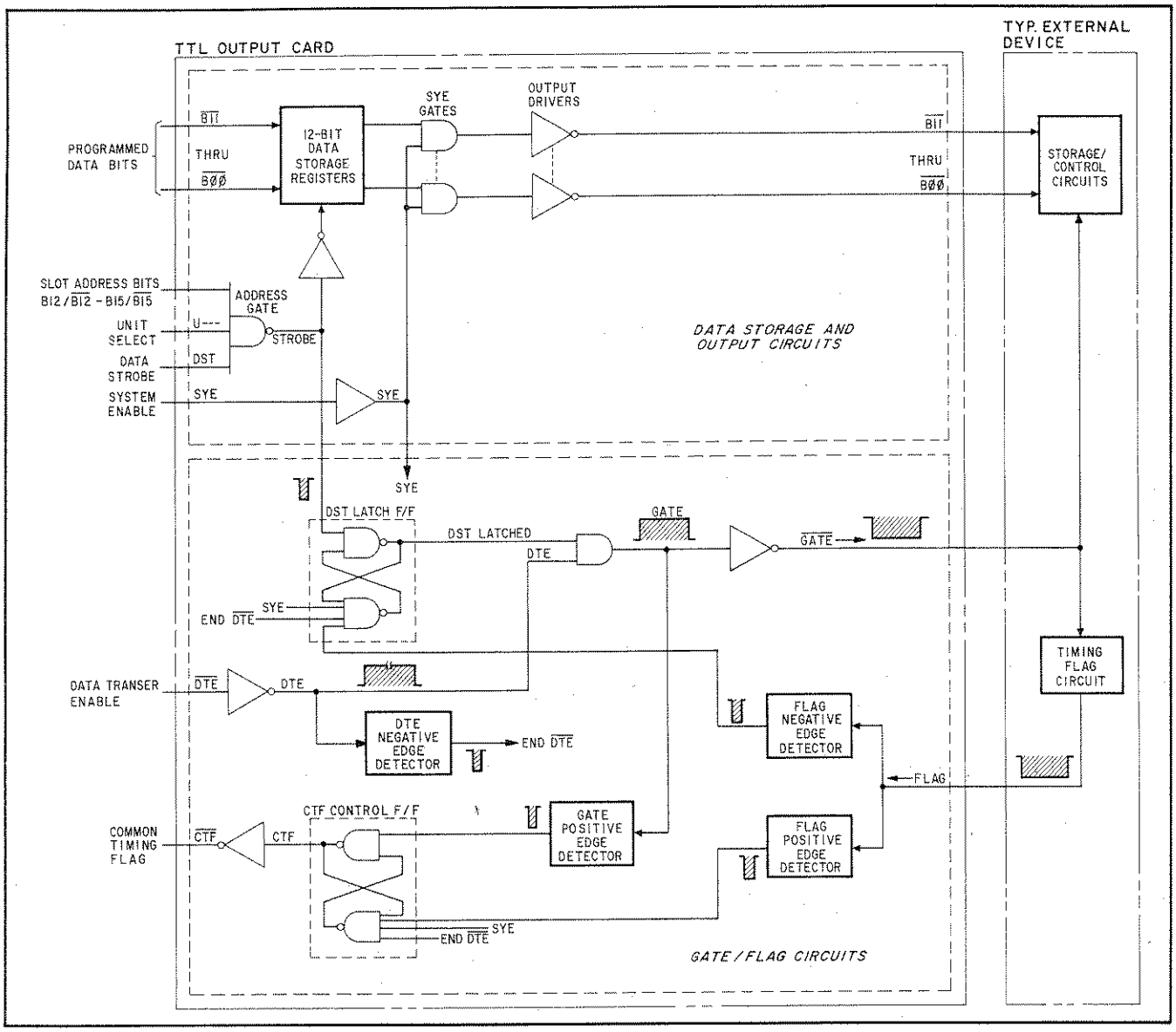


Figure 4-1. Output Card, Model 69331A, Block Diagram

4-1 INTRODUCTION

4-2 This section contains principles of operation for TTL Output Card, Model 69331A. Theory is presented on both a block diagram and a detailed circuit theory level.

4-3 BLOCK DIAGRAM THEORY

4-4 Figure 4-1 is a block diagram of the TTL output card. The card consists of two essentially independent circuit groups: a data storage and output circuits group which stores programmed data

and provides a bit-pattern output that is either identical to (standard 69331A card) or the complement of (Option 073) the programmed bit pattern; and a gate/flag circuit which, in response to a programmed DTE mode bit, signals the external device that new data is available on the card output, and also accepts a device FLAG signal which controls the busy/ready status of the $\overline{CTF}$ line returned to the multiprogrammer (and ultimately to the computer).

4-5 DATA STORAGE AND OUTPUT CIRCUITS

4-6 This circuit group consists of an address gate circuit, a strobe amplifier, a 12-bit data storage register, a set of 12 AND gates and output drivers, and an SYE circuit. When the output card slot is addressed, the slot address bits all go to the HI state. If the unit containing the card has been selected by a previous control word, U-- is also HI. When a DST pulse appears, a positive strobe pulse, the width of DST, is generated and applied to the data storage registers and the gate/flag circuit. The strobe pulse enters data bits $\overline{B\emptyset\emptyset}$ through $\overline{B11}$ into local storage. The outputs of the storage flip-flops are applied to the AND gates, and if SYE has been programmed, the stored bits are coupled to the output drivers. The drivers amplify and invert the stored data and transfer it to the output connector.

4-7 GATE/FLAG CIRCUIT

4-8 A timing diagram of the signals generated by the GATE/FLAG circuit is given in Figure 4-2 and described as follows:

T_0 - At T_0, the multiprogrammer is initially turned on and SYE has not yet been programmed. The LO SYE line holds the DST latch and CTF control F/F's in the reset state. This insures that the $\overline{GATE}$ and $\overline{CTF}$ lines remain in the reset (off) state until after SYE has been programmed.

T_1 - SYE is programmed on (SYE goes HI) releasing the DST latch and CTF control F/F's.

T_2 - The card is addressed and strobed. The DST latch F/F is set (DST LATCHED goes HI).

T_3 - DTE is programmed. The two functions (DTE and DST LATCHED) enable an AND gate, the output of which is amplified and inverted to become the $\overline{GATE}$ output of the card. The start of this function (DTE · DST LATCHED) is also detected and used to set the CTF control flip-flop. With the CTF control flip-flop set, the $\overline{CTF}$ line goes to the LO (busy) state.

T_4 - The $\overline{GATE}$ output starts an external timing flag circuit and this circuit returns a device $\overline{FLAG}$ signal to the card. Following a short delay, the flag negative-edge detector circuit generates a negative pulse. This pulse resets the DST LATCH F/F which in turn resets the $\overline{GATE}$ line in preparation for the next DTE cycle.

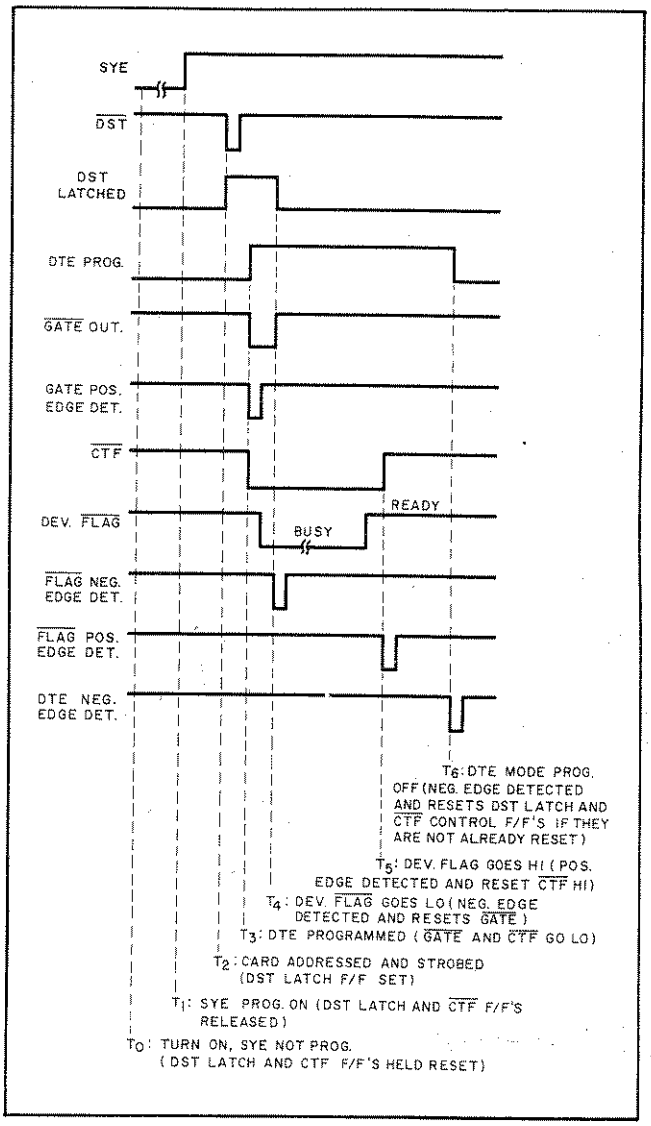


Figure 4-2. GATE/FLAG Circuit, Timing Diagram

T_5 - As long as the device $\overline{FLAG}$ is in the busy state, the $\overline{CTF}$ line is also held in the busy state. When the external circuit times out (T_5) the device $\overline{FLAG}$ line goes HI. The flag positive-edge detector responds to this transition by generating a negative pulse which resets the CTF control flip-flop. $\overline{CTF}$ is now returned to the ready (HI) state.

T_6 - When the DTE mode is programmed off, a DTE negative-edge detector responds to this transition and generates a negative pulse. This pulse will reset the DST latch and CTF control flip-flops if they have not been already reset by the device $\overline{FLAG}$ return signal. This is actually a back-up function which enables the gate/flag circuit to be cleared in the event the external device fails to return a $\overline{FLAG}$ signal.

4-9 DETAILED CIRCUIT ANALYSIS (See Figure 7-1)

4-10 DATA STORAGE AND OUTPUT CIRCUITS

4-11 Addressing. When the slot and unit in which the output card is housed are addressed, the four address bits and U-- go HI. Data bits $\overline{B11}$ through $\overline{B\emptyset\emptyset}$ are also present at this time but are not yet entered into storage. Approximately 4μsec after the programmed word appears, a data strobe pulse (DST) is received by the output card. The 4μsec delay of DST allows the data lines to settle before the data is stored. When DST appears, it enables NAND gate Z10 which in turn produces a negative pulse the width of DST. Transistor Q1 inverts the negative pulse and applies it to the 12-bit data storage register and the gate/flag circuit.

4-12 Data Storage. The 12-bit data storage register is comprised of six two-bit storage flip-flops (Z1 through Z6). The individual stages are D-type, positive-edge triggered flip-flops. The logical state at the D-input of a flip-flop is transferred to the Q output terminal when the clock terminal (CLK) is strobed by a positive-going pulse. ($\overline{Q}$ always assumes the state opposite the Q state.) When a bit is programmed to a logical 1 at the computer, the corresponding B-- data lines goes LO. The strobe pulse from Q2 transfers this LO level from the D-input to the Q output ($\overline{Q}$ of course goes HI). The stored bits are taken from the $\overline{Q}$ side of the flip-flops and will therefore be the complement of the input data. Each stored bit is applied to either an AND gate (standard 69331A) or a NAND gate (Option 073).

4-13 SYE Logic Gates. Logic gates Z7, Z8, and Z9 will pass the stored data bits to the output driver transistors whenever SYE is programmed on (HI). For the standard card, the stored bits will be passed to the output drivers uninverted; for Option 073 the bits will be inverted.

4-14 Output Drivers. Output drivers A1 through A12 are each composed of a single inverting amplifier stage. As supplied from the factory (jumper J4 to A), the collector voltage for the drivers is derived from the +5 volt multiprogrammer supply and the output bit levels will therefore switch between 0 and +5 volts. Two additional options allow the drivers to be operated from a nominal 12 volt collector supply or as open collector drivers (see Paragraph 3-14).

4-15 GATE/FLAG CIRCUITS

4-16 The gate numbers shown within the logic symbols in Figure 7-1 (e. g. G1) are for reference in tracing circuit operation; they have no physical relationship to the actual parts. The Z numbers adjacent to the gates, however, are the actual reference designations of the IC's and these numbers are etched on the printed circuit card, for physical location of the IC's.

4-17 Detailed circuit operation is described for the following phases of operation:

a. Initial Turn on
b. Start-of-GATE and $\overline{CTF}$
c. Start-of-Flag
d. End-of-Flag
e. End-of-DTE.

4-18 Initial Turn On. When the multiprogrammer system is first turned on, and before SYE has been programmed on, transistor Q5 is cut off and its collector voltage is at a HI level. This level is applied to the base of transistor Q6, switching Q6 on. The LO collector voltage of Q6 holds the DST LATCH and CTF CONTROL flip-flops in the reset state. Once SYE is programmed on it goes HI, releasing the two flip-flops.

4-19 Start-of-Gate and $\overline{CTF}$. Each time data is strobed into storage, and provided SYE has been programmed on, one condition for generating a $\overline{GATE}$ output and setting the $\overline{CTF}$ line LO is satisfied; that of latching the data strobe. The second condition requires that the data transfer enable mode be programmed on ($\overline{DTE}$, LO). When the data strobe pulse appears, the output of address gate Z10 goes LO for the period of DST (approximately 1μsec) and sets the DST LATCH flip-flop. The resulting HI output of gate G1 is applied as one input to NAND gate G3. The second input to G3 is derived from $\overline{DTE}$, and is coupled through emitter-follower Q2 and inverter G10 to G3. With DST latched and DTE programmed on, both inputs to NAND gate G3 are HI. The LO output of G3 ($\overline{DST\ LATCHED \cdot DTE}$) is inverted by gate G4, amplified and inverted by Q3, and applied to output pin 13 as $\overline{GATE}$.

4-20 The initial negative transition of $\overline{DST\ LATCHED \cdot DTE}$ is detected by the circuit consisting of G4, G5, R10, and C9, and it generates a short-duration negative pulse coincident with this transition. (Operation of the detector circuit is described in the next paragraph.) The negative pulse sets the CTF CONTROL flip-flop and its output goes HI. CTF is inverted by transistor Q4, setting $\overline{CTF}$ to the LO (busy) state.

4-21 The start of DST and DTE detector makes use of the discharge time of capacitor C9 to generate a negative set pulse for the CTF CONTROL flip-flop. At the time $\overline{DST\ LATCHED \cdot DTE}$ initially goes LO, capacitor C4 begins to discharge, but, since it cannot discharge instantaneously, it temporarily holds one input to NAND gate G5 HI. Gate G4 inverts $\overline{DST\ LATCHED \cdot DTE}$, and this holds the second input to NAND gate G5 HI. The resulting

LO output of G5 resets the CTF CONTROL flip-flop. When C9 has discharged to the LO level, NAND gate G5 is inhibited and its output returns HI.

4-22 Start-of-Flag. In response to the $\overline{\text{GATE}}$ output going LO, the external device will return a $\overline{\text{FLAG}}$ signal to the TTL card. The $\overline{\text{FLAG}}$ input is first terminated by resistors R17 and R18 and then inverted three times by gates G18, G17, and G16. The R-C network consisting of resistors R14 and R15 and capacitor C12 provides a 1μsec delay of the FLAG signal and reduces the susceptibility of the input circuit to transients. Resistor R9, connected between the output of G16 and the input of G17, provides hysteresis to prevent oscillation with the increased input rise time of Z15.

4-23 The HI output of gate G16 is applied to start-of-flag detector G15, G13, R12 and C6. (The operation of this circuit is similar to that described for the start of DST and DTE circuit in Paragraph 4-20.) The negative start-of-flag pulse at the output of G13 is propagated through gates G8 and G9 and resets the DST latch flip-flop. The output of flip-flop gate G1 now goes LO and inhibits NAND gate G3. The HI output of G3 causes the $\overline{\text{GATE}}$ output to go HI.

4-24 End-of-Flag. When the external timing circuit times out, the $\overline{\text{FLAG}}$ input signal to the TTL card goes HI. The end-of-flag circuit consisting of G15, G14, R13, and C11 senses the input LO-to-HI transition and generates a negative pulse which resets the CTF CONTROL flip-flop and returns the $\overline{\text{CTF}}$ line to the ready (HI) state.

4-25 End-of-DTE. When the DTE mode is terminated, the input to the end-of-DTE pulse generator (G11, G12, R11, and C8) makes a transition from a HI to a LO-level. This transition is sensed by the pulse generator and it generates a negative pulse which resets the CTF CONTROL and DST LATCH flip-flops.